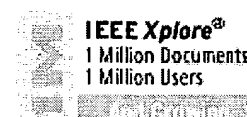


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instruction length decode

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Roncken, M.; Stevens, K.; Pendurkar, R.; Rotem, S.; Chaudhuri, P.P.; Advanced Research in Asynchronous Circuits and Systems, 2000. (ASYNC 2000) Proceedings. Sixth International Symposium on , 2-6 April 2000  
Pages:62 - 72

[\[Abstract\]](#) [\[PDF Full-Text \(160 KB\)\]](#) IEEE CNF**2 Synthesis of asynchronous control circuits with automatically generated relative timing assumptions**

Cortadella, J.; Kishinevsky, M.; Burns, S.M.; Stevens, K.; Computer-Aided Design, 1999. Digest of Technical Papers. 1999 IEEE/ACM International Conference on , 7-11 Nov. 1999  
Pages:324 - 331

[\[Abstract\]](#) [\[PDF Full-Text \(860 KB\)\]](#) IEEE CNF**3 Bounding average time separations of events in stochastic timed Petri nets with choice**

Aiguo Xie; Sangyun Kim; Beerel, P.A.; Advanced Research in Asynchronous Circuits and Systems, 1999. Proceedings., Fifth International Symposium on , 19-21 April 1999  
Pages:94 - 107

[\[Abstract\]](#) [\[PDF Full-Text \(352 KB\)\]](#) IEEE CNF**4 CAD directions for high performance asynchronous circuits**

Stevens, K.; Rotem, S.; Burns, S.M.; Cortadella, J.; Ginosar, R.; Kishinevsky, K.; Roncken, M.;

Design Automation Conference, 1999. Proceedings. 36th , 21-25 June 1999  
Pages:116 - 121

[\[Abstract\]](#) [\[PDF Full-Text \(528 KB\)\]](#) IEEE CNF**5 RAPPID: an asynchronous instruction length decoder**

Rotem, S.; Stevens, K.; Ginosar, R.; Beerel, P.; Myers, C.; Yun, K.; Kol, R.; Dike, C.; Roncken, M.; Agapie, B.; Advanced Research in Asynchronous Circuits and Systems, 1999. Proceedings., Fifth International Symposium on , 19-21 April 1999  
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**1 A 500 MHz 32b 0.4  $\mu$ m CMOS RISC processor LSI**
*Suzuki, K.; Yamashina, M.; Nakayama, T.; Izumikawa, M.; Nomura, M.; Igura, H.; Heiuchi, H.; Goto, J.; Inoue, T.; Koseki, Y.; Abiko, H.; Okabe, K.; Ono, A.; Yano, Y.; Yamada, H.;*

 Solid-State Circuits Conference, 1994. Digest of Technical Papers. 41st ISSCC., 1994 IEEE International , 16-18 Feb. 1994  
 Pages:214 - 215

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**Design Alternatives for Barrel Shifters - Matthew Pillmeier Rushmore (2002) (Correct)**  
Design alternatives for barrel shifters Matthew R. Pillmeier Rushmore Processor 2 Bethlehem, Pa 18015, Usa Abstract Barrel Shifters Are Often Utilized By embedded Digital Signal paper examines design alternatives for barrel shifters that perform the following functions: shift [www.eecs.lehigh.edu/~caar/papers/SPIE2002\\_Shifter.pdf](http://www.eecs.lehigh.edu/~caar/papers/SPIE2002_Shifter.pdf)

**Fault-Secure Shifter Design: Results and Implementations - Ricardo Duarte Nicolaidis (1997) (Correct)**  
to the first input of the first FPS and one to the second input of the first FPS (as shown in figure 9a. Fault-Secure Shifter Design: Results and Implementations Ricardo O. requirements for the design of self-checking shifters and is part of a broader project concerning the galahad.informatik.tu-chemnitz.de/proceedings/edit/papers/1997/ed97/htmlfiles/sun\_sgi/./pdffiles/06b\_2.pdf

**Hardware Supported Simulation System for Graphs - Hartmann, (Correct)**  
t CLOCK = 32ns the number of cell operations per second will be 10 9 This architecture is easy Subgraph Matching within Cellular Hypergraphs. Second International Conference on Developments in xyz-memory holding one generation, 2) a xy-plane shifter, 3) a line array shifter, 4) a computing [www.isa.informatik.th-darmstadt.de/MP/Publikationen/acri98b.ps](http://www.isa.informatik.th-darmstadt.de/MP/Publikationen/acri98b.ps)

**Statistically Optimized Asynchronous Barrel Shifters for - Beereel, Kim, Yeh, Kim (1999) (Correct) (1 citation)**  
This paper presents low-power asynchronous barrel shifters for variable length encoders and decoders useful is to create multi-level asynchronous barrel shifters optimized for the skewed shift control [jungfrou.usc.edu/pub/islped99.ps](http://jungfrou.usc.edu/pub/islped99.ps)

**Development of Triadic Neural Circuits for Visual Image - Gupta, Alley, Marshall (1998) (Correct)**  
but before calculation of the inhibition. The second learning step was performed after the winner had by eye movements. The development of a neural shifter circuit (Oshausen, Anderson, Van Essen, 1992) The triadic learning rule thus produces a shifter circuit that exhibits visual image [www.cs.unc.edu/Research/brainlab/PAPERS/shift9807.ps.gz](http://www.cs.unc.edu/Research/brainlab/PAPERS/shift9807.ps.gz)

**A Low-Power 32 bit Datapath Design - Heo (2000) (Correct) (1 citation)**  
every cycle, the maximum possible activity, the second sequence (0110011001) has one transition possible input and internal state combination. Second, it is not flexible. If we need to change some area-efficient logic unit design. Also, we explore shifter designs - a simple but essential block in the [www.cag.fcs.mit.edu/scale/papers/heomoo-sm.pdf](http://www.cag.fcs.mit.edu/scale/papers/heomoo-sm.pdf)

**Qiang Xie and Daniel Gajski - January Center For (Correct)**  
out of five allocated buses only four are mapped. Secondly, when we allocate registers for all the 4. Experimental Results 4.4.1 Design 1: 1 ALU, 1 Shifter, 1 RF, 3 buses . 5.4.2 Design 2: 1 ALU, 1 Shifter, 4 registers, 3 buses [www.eecs.uci.edu/technical\\_report/TR02-06.pdf](http://www.eecs.uci.edu/technical_report/TR02-06.pdf)

**Leading-One Prediction Scheme for Latency Improvement in - Bruguera, Lang (1998) (Correct) (1 citation)**  
carried out in parallel with the encoding and the second as part of the normalization shifting. 4.1. during the first stage and to apply it in the second. For the delay of the correction mux and the University Of California At Irvine Input B Result Shifter Shifter Result Shift Coding Shift Coding Input A [www.ac.usc.es/files/articulos/1998/gact1998-c04.ps.gz](http://www.ac.usc.es/files/articulos/1998/gact1998-c04.ps.gz)

**An EPLD Based Transient Recorder for Simulation of Video - Larsson University (Correct)**  
Fadc Vdac Epd Epn7128 Epd Epn7128 Controller Shifter 32 X 1m Dram (simm) Videocout Videoin Vdac.vhdl of the transient recorder. One of these EPLDs (shifter) implements a 4 1 Theta 8 bit wide video shift

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**Waveguide Type Rotating Phase Plate as Optical Frequency - Hiroaki Inoue Shinji (1994) (Correct)**  
Type Rotating Phase Plate as Optical Frequency Shifter Hiroaki Inoue, Shinji Nishimura, Tatsuo technology. Here, an optical frequency shifter would be one of the most important devices, of waveguide type optical frequency shifter based on the rotating phase plate, as our [jisp.cs.nyu.edu/RWC/rwcp/papers/1994/B-08\\_155.ps.gz](http://jisp.cs.nyu.edu/RWC/rwcp/papers/1994/B-08_155.ps.gz)

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of the shift register and buffer register of the shifter EPLD (fig. 4)A video operational amplifier tech-[www.informatik.uni-hamburg.de/Personal/larsson/papers/epkltan\\_springer\\_incs1142.ps.gz](http://www.informatik.uni-hamburg.de/Personal/larsson/papers/epkltan_springer_incs1142.ps.gz)

**Reduction of 3rd Order Intermodulation of a Semiconductor Laser - Steiner (Correct)**  
path with a cubic law device, an adjustable phase shifter and an adjustable attenuator. Using such a because of the amplitude deviation of the phase shifter these requirements are hard to meet. II. NEW Topology And Experimental Results Adding A Phase Shifter And An Attenuator To The Linear Path Improves [www.ihf.ee.ethz.ch/~ornl/PDF\\_Paper/Guido\\_Topical\\_PDF.pdf](http://www.ihf.ee.ethz.ch/~ornl/PDF_Paper/Guido_Topical_PDF.pdf)

**Application of the ANNA Neural Network Chip to - Sackinger, Boser, (1992) (Correct) (13 citations)**  
chip is capable of processing 1,000 characters per second. The recognition system has essentially the same evaluates a maximum of 10 #10 9 connections per second #10 GC=8# corresponding to 8 neurons#258 4K On Chip Weight Memory Neuron Function: Barrel Shifter z =(f wx i i Input State Vector x 8 [home.talkcity.com/LaGrangeLn/sackinger/public/tmn92.pdf](http://home.talkcity.com/LaGrangeLn/sackinger/public/tmn92.pdf)

**The Amplitude and Phase Control of the ALS Storage Ring RF System - Lo Taylor And (Correct)**  
And Phase Loops Of The Als Sr Rf System Phase Shifter Klystron Drive Controller Klystron Phase Servo Since the RF signal must go through a phase shifter, a couple of amplifiers, an electronic Respectively. Output From Feeder Waveguide Phase Shifter Phase Detector From Master Oscillator Input [www.aps.anl.gov/conferences/mirrored/www.cern.ch/accelconf/p85/ARTICLES/TAR/TAR03.PDF](http://www.aps.anl.gov/conferences/mirrored/www.cern.ch/accelconf/p85/ARTICLES/TAR/TAR03.PDF)

**Circuit Techniques for 1.5-V Power Supply Flash Memory - Nobuaki Otsuka And (Correct)**  
a 0- signal to a differential 0- output, while the second level shifter takes the 0signal and generates a The switching speed of the input signals for the second shifter, and is slow because of the switching and the memory core circuits, two types of level shifter circuits are proposed which convert a VDD level [mos.stanford.edu/papers/no\\_jssc\\_97.pdf](http://mos.stanford.edu/papers/no_jssc_97.pdf)

**Floating Point Unit Generation and Evaluation for FPGAs - Jian Liang And (Correct)**  
contains a subtractor. The normalizer requires a second shifter to convert the resulting number into are fed into the exponent comparator. In the pre-shifter, a new mantissa is created by right shifting the and the exponent is increased 1-Bit Possible Shifter Exponent Correction Result Exponent Result [www.eecs.umass.edu/eece/lessier/jliang-fcm03.pdf](http://www.eecs.umass.edu/eece/lessier/jliang-fcm03.pdf)

**Mutable Functional Units: Initial Results - Solihin, Cameron, Luo, (Correct)**  
stage (align) contains a right shifter, the second (add) contains a 54-bit adder, and the third and oating-point addition/subtraction. Second, the 53bit right shifter is replaced by a 64-bit and logic unit (ALU)integer multiplier, integer shifter, oating-point adder, multiplier/divider, [iacoma.cs.ucluc.edu/~solihin/Paper/mfu\\_fcm01.ps](http://iacoma.cs.ucluc.edu/~solihin/Paper/mfu_fcm01.ps)

**Decoupling Change from Design - VanHilst, Notkin (1996) (Correct) (11 citations)**  
modularization but rather to augment it with a second level of modularization where the standard of modularization but rather to augment it with a second, lower level of modularization. As will be seen, had five modules-line storage, input, circular shifter, alphabetizer, and output. The dominant reason [www.cs.washington.edu/homes/vanhilst/tse60l.ps.gz](http://www.cs.washington.edu/homes/vanhilst/tse60l.ps.gz)

**Low-Swing Clock Domino Logic Incorporating Dual Supply - Seong-Ook Jung, (Correct)**  
the delay time from input to dynamic node and the second term represents the delay time from dynamic node delay increase by 2 (or, Deltad V dd (y) 2)Second, if a gate (say u) lowers its supply voltage, Flow L VddL VddH (a) DC Current Path (b) Level Shifter INv with VddL L Figure 1: DC current and level [www.cs.ucla.edu/~mnivero/PAPER/p467-jung.pdf](http://www.cs.ucla.edu/~mnivero/PAPER/p467-jung.pdf)

**Influence of Radiation Damage on the Performance - Of Lead Scintillator (Correct)**  
and 20 Gy/h, respectively. In order to achieve secondary electron equilibrium thin plastic sheets were 10 is the effective fluorescence light yield. The second term in eq. 1) describes the reflection of electrons. Plastic scintillators and wavelength shifter bars were irradiated uniformly with #rays. Both [maren.desy.de/englisch/veroeffentlichungen/././veroeffentlichungen/testbeam\\_scrip12.ps](http://maren.desy.de/englisch/veroeffentlichungen/././veroeffentlichungen/testbeam_scrip12.ps)

**Optimization of Photodiode Readout of Csl(Tl) Crystals - Brose Dahlinger Eckstein (1995) (Correct)**  
but increases it by a factor of 1.5 only. The second photodiode does not transfer all absorbed light whereas a reflecting material at position of the second photodiode redirects a part of the light to the different readout schemes (direct and wavelength shifter)The linearity of the system and two

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Register Relocation: Flexible Contexts for Multithreading - Waldspurger, Wehl (1993) (Correct) (29 citations)

relocation hardware should affect only the instruction decode stage of the processor pipeline, and hardware should affect only the instruction decode stage of the processor pipeline, and would be a table describes the experimental parameters. The second table lists the cost assumptions used for both

www.research.digital.com/SRC/personal/Carl\_Waldspurger/papers/register-isca93.ps

Computer Design Strategy for MCM-D/Flip-Chip Technology - Franzon, al. (Correct)

to build a 'MegaChip' CPU consisting of an Instruction Fetch Unit and Execution Unit. By building connection is 9 mm. The I-Cache to instruction/Decode unit input register path thus has a total length

www.ece.ncsu.edu/info.ece/vlsi\_info/techreports/NCSU-ERL-98-03.PS.Z

Comparing Software and Hardware Schemes For Reducing the... - Hwu, Conte, Chang (1989) (Correct) (16 citations)

a common technique to increase throughput of the instruction fetch, instruction decode, and instruction

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Systematic Prototyping of Superscalar Computer Architectures - Thomas Conte (1992) (Correct) (3 citations)

that use inputs composed of a set of traces of instructions taken from executing programs. These traces of two phases: instruction fetch and instruction decode. The instruction fetch phase fetches instructions runs for 1.30 minutes on a 20 million instructions/second machine executes 1.8 billion instructions. The

www.tinker.ncsu.edu/contel/rsp92.ps

Wrong-Path Instruction Prefetching - Pierce, Mudge (1994) (Correct) (25 citations)

Wrong-Path Instruction Prefetching Jim Pierce 1 and Trevor Mudge

www.eecs.umich.edu/techreports/cse/1994/CSE-TR-222-94.ps.gz

From Algorithm Parallelism to Instruction-Level Parallelism: An... - Vishkin (1997) (Correct) (4 citations)

From Algorithm Parallelism to Instruction-Level Parallelism: An Encode-Decode Chain

www.umiacs.umd.edu/users/Vishkin/PUBLICATIONS/spaa97.ps

A TRS Model for a Modern Microprocessor Computation Structures - Poyneer, Hoe, Arvind (Correct)

And Arvind June 25, 1998 1 Background The Ax Instruction Set, A Minimalist Risc Isa, Was Described By are fetched from the memory and sent to the decode unit. The BTB provides predictions of the next

csg-ftp.cs.mit.edu/pub/papers/csgmemo/memo-408.ps.gz

Zero-Cycle Loads: Microarchitecture Support for Reducing Load... - Austin (1995) (Correct) (31 citations)

Abstract Untolerated load instruction latencies often have a significant impact on

for pipelines with a single stage of instruction decode, and another for pipelines with multiple decode

ftp.cs.wisc.edu/sohi/papers/1995/micro.zcl.ps.gz

Branch History Table Indexing to Prevent Pipeline Bubbles in... - Tse - Yu Yeh (1993) (Correct) (3 citations)

predictor, a superscalar processor must predict instruction fetch addresses no later than the first

www.eecs.umich.edu/HPS/pub/micro-93.bht-indexing.ps

Simulation of Asynchronous Instruction Pipelines - Chia-Hsing Chien (1996) (Correct)

Simulation Conference Simulation of Asynchronous Instruction Pipelines Chia-Hsing Chien Mark A. Franklin

www.cs.wustl.edu/cs/techreports/1996/wucs-96-05.ps.Z

The Pendulum Instruction Set Architecture (PISA) - Carlin Vieri (Correct)

The Pendulum Instruction Set Architecture (PISA) Carlin Vieri May 5,

www.ai.mit.edu/~cvieri/pisa.ps

Instruction Decode and Operand Fetch Process of ECSTAC-P - Morton, al. (1994) (Correct)  
Electronic Mail: mort@eleceng.adelaide.edu.au Instruction Decode and Operand Fetch Process of ECSTAC-P  
Mail: mort@eleceng.adelaide.edu.au Instruction Decode and Operand Fetch Process of ECSTAC-P by Shannon  
register) only occurs on either the first and/or second bytes of each instruction (never the third or  
www.eleceng.adelaide.edu.au/Groups/CHIPTEC/papers/HPCA-ECS-94-02.ps

Issues in Partitioning Integrated Circuits for... - Sanjeev Banerjee (1996) (Correct) (1 citation)  
Data Queue Address Data and FPU Integer Unit Instruction Unit Memory Management Unit 32 128 128 Result  
advantages to be gained Machine State Unit PC Decode Issue Branch Resolution External Interrupt  
www.ece.ncsu.edu/info.ece/vlsi\_info/techreports/NCSU-ERL-98-02.PS.Z

Design Alternatives for Barrel Shifters - Matthew Pillemeier Rushmore (2002) (Correct)  
Design alternatives for barrel shifters Matthew R. Pillemeier Rushmore Processor 2  
Bethlehem, Pa 18015, Usa Abstract Barrel Shifters Are Often Utilized By embedded Digital Signal  
paper examines design alternatives for barrel shifters that perform the following functions: shift  
www.eecs.tehigh.edu/~caar/papers/SPIE2002\_Shifter.pdf

Real-Time Mpeg-2 Software Decoding With A Dual-Issue... - Holmann, Yarnada... (1996) (Correct)  
(VLD) and block loading processes a 32KB instruction RAM and a 16KB data RAM. The VLD hardware  
bi-directionally predicted non-intra blocks are decoded in less than 800 cycles, leading to a single  
its first operand with the high half-word of its second operand. For many applications, this effectively  
nova.stanford.edu/~edgar/papers/vls96.ps.gz

Sequencing Run-Time Reconfigured Hardware with Software - Wirthlin (1996) (Correct) (24 citations)  
for configuration at run-time. The Dynamic Instruction Set Processor (DISC)3 is a run-time  
module eliminates the instruction fetch, decode, and other overhead associated with general  
splish.ee.byu.edu/docs/lpg98\_final.ps.gz

Fault-Secure Shifter Design: Results and Implementations - Ricardo Duarte Nicolaidis (1997) (Correct)  
(VLD) and block loading processes a 32KB instruction RAM and a 16KB data RAM. The VLD hardware  
Fault-Secure Shifter Design: Results and Implementations Ricardo O.  
requirements for the design of self-checking shifters and is part of a broader project concerning the  
galahad.informatik.tu-chemnitz.de/proceedings/edtc/papers/1997/edt97/htmlfiles/sun\_sgl/.../pdffiles/06b\_2.pdf

Identifying Contributing Factors to ILP - González, González (1996) (Correct)  
This paper presents a thorough study of the instruction level parallelism that can be exploited by  
which have an ILP bounded by 4 due to the fetch, decode and/or issue width, are far beyond the limits  
previous memory references have been issued. The second scheme (called in-order) assumes that if a memory  
ftp.ac.upc.es/pub/reports/CEPBA/1996/UPC-CEPBA-1996-12.ps.Z

Hardware Supported Simulation System for Graph... - Hartmann... (Correct)  
t CLOCK =32ns the number of cell operations per second will be 10 9 This architecture is easy  
xyz-memory holding one generation, 2) a xy-plane shifter, 3) a line array shifter, 4) a computing  
2) a xy-plane shifter, 3) a line array shifter, 4) a computing window and (5) p processing  
www.isa.informatik.th-darmstadt.de/MP/Publikationen/acri96b.ps

Performance Advantages Of Merging Instruction- And... - Quintana, Espasa, Valero (1998) (Correct)  
Performance Advantages Of Merging Instruction- And Datalevel Parallelism (extended Version)  
ftp.ac.upc.es/pub/reports/DAC/1998/UPC-DAC-1998-43.ps.Z

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Register Relocation: Flexible Contexts for Multithreading - Waksdurger, Wehl (1993) (Correct) (29 citations)

relocation hardware should affect only the instruction decode stage of the processor pipeline, and hardware should affect only the instruction decode stage of the processor pipeline, and would be a table describes the experimental parameters. The second table lists the cost assumptions used for both

www.research.digital.com/SRC/personal/Carl\_Waksdurger/papers/register-isca93.ps

Computer Design Strategy for MCM-D/Flip-Chip Technology - Franzon, al. (Correct)

to build a 'MegaChip' CPU consisting of an Instruction Fetch Unit and Execution Unit. By building connection is 9 mm. The I-Cache to Instruction/Decode unit input register path thus has a total length

www.ece.ncsu.edu/info.ece/visi\_info/techreports/NCSU-ERL-96-03.PS.Z

Comparing Software and Hardware Schemes For Reducing the... - Hwu, Conte, Chang (1989) (Correct) (16 citations)

a common technique to increase throughput of the instruction fetch, instruction decode, and instruction

ftp.crlc.uiuc.edu/pub/IMPACT/conference/isca-89-branch.ps

Tr-93-08-08 - Wayne State University (Correct)

:ng. The permutation with the symbol 2 at the second position is reached, after this sequence of

Embedding of cycles in rotator and incomplete rotator graphs Subburajan Ponnuswamy and Vipin

Embedding of cycles in rotator and incomplete rotator graphs Subburajan Ponnuswamy and Vipin

www.pdcl.eng.wayne.edu/tech\_reports/tr-93-08-08.ps

Systematic Prototyping of Superscalar Computer Architectures - Thomas Conte (1992) (Correct) (3 citations)

that use inputs composed of a set of traces of instructions taken from executing programs. These traces

of two phases: instruction fetch and instruction decode. The instruction fetch phase fetches instructions

runs for 1:30 minutes on a 20 million instructions/second machine executes 1.8 billion instructions. The

www.tinker.ncsu.edu/contc/isp92.ps

Wrong-Path Instruction Prefetching - Pierce, Mudge (1994) (Correct) (25 citations)

Wrong-Path Instruction Prefetching Jim Pierce 1 and Trevor Mudge

www.eecs.umich.edu/techreports/cse/1994/CSE-TR-222-94.ps.gz

From Algorithm Parallelism to Instruction-Level Parallelism: An... - Vishkin (1997) (Correct) (4 citations)

From Algorithm Parallelism to Instruction-Level Parallelism: An Encode-Decode Chain

www.umiacs.umd.edu/users/vishkin/PUBLICATIONS/spaa97.ps

A TRS Model for a Modern Microprocessor Computation Structures - Poyneer, Hoo, Arvind (Correct)

And Arvind June 25, 1998 1 Background The Ax Instruction Set, A Minimalist Risc Isa, Was Described By

are fetched from the memory and sent to the decode unit. The BTB provides predictions of the next

csg-ftp.lcs.mit.edu/pub/papers/csgmemo/memo-408.ps.gz

Zero-Cycle Loads: Microarchitecture Support for Reducing Load... - Austin (1995) (Correct) (31 citations)

Abstract Untolerated load instruction latencies often have a significant impact on

for pipelines with a single stage of instruction decode, and another for pipelines with multiple decode

ftp.cs.wisc.edu/sohi/papers/1995/micro.zcl.ps.gz

Performance Of The QZ Algorithm In The Presence Of Infinite... - Watkins (2000) (Correct) (4 citations)

a nonzero entry in the lower triangle of B. The second rotator then restores B to upper triangular form.

consists of a sequence of pairs of Givens rotators, the first of which annihilates an entry of A

entry in the lower triangle of B. The second rotator then restores B to upper triangular form. It is

www.sci.wsu.edu/math/faculty/watkins/profiles/qzinf.ps

Tr-93-03-03 - Wayne State University (Correct)  
Embedding of Meshes on Rotator Graphs Subburajan Ponnuswamy and Vipin  
Faculty Research Award Embedding of Meshes on Rotator Graphs Subburajan Ponnuswamy and Vipin  
-A set of directed permutation graphs called rotator graphs were proposed as an alternative to the  
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Tr-93-04-04 - Wayne State University (Correct)  
from the source node of the message. Since the second symbol of all the permutations at level two is  
Low latency routing algorithms for rotator and star networks Subburajan Ponnuswamy and  
Award. Low latency routing algorithms for rotator and star networks Subburajan Ponnuswamy and  
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Branch History Table Indexing to Prevent Pipeline Bubbles in... - Tse--Yu Yeh (1993) (Correct) (3 citations)  
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www.eecs.umich.edu/~hps/pub/micro-93.bht-indexing.ps

Super Rotator: Incrementally Extensible Directed Network Graph of... - Srimani (1996) (Correct)  
graphs (components of the different classes)The second term accounts for all the type A edges for any  
Computer Science Technical Report Super Rotator: Incrementally Extensible Directed Network Graph  
491-2466 WWW: www.cs.colostate.edu Super Rotator: Incrementally Extensible Directed Network Graph  
www.cs.colostate.edu/~hpspub/TechReports/1996/tr96-116.ps.Z

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www.eleceng.adelaide.edu.au/Groups/CHIPTEC/papers/HPCA-ECS-94-02.ps

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www.ece.ncsu.edu/info.ece/visi\_info/techreports/NCSU-ERL-96-02.PS.Z

Helical spin rotators and snakes for RHIC - Plitsin And Yu (Correct)  
caused by the first pair is compensated by the second. Asserting that magnets of each pair have the  
Helical spin rotators and snakes for RHIC V.I.Plitsin and  
NY 11973, USA Abstract Various possible spin rotator and siberian snake schemes are considered for  
accelconf.web.cern.ch/AccelConf/p95/ARTICLES/RAQ/RAQ21.PDF

Tr-93-07-07 - Wayne State University (Correct)  
1 3 c, m 2 =b nq2 \Gamma\_2 2 3 c, and the second summation is zero for d =1 and 2. Proof: Given  
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Award. A comparative study of star graphs and rotator graphs Subburajan Ponnuswamy and Vipin  
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